DESIGN AND FABRICATION OF AN ANALOG VOLTAGE TO DUTY CYCLE GENERATOR

SIXTH INTERIM PROGRESS REPORT

October 1967

Contract No. NAS7-100
Task Order Number RD-28
JPL Contract Number 951306

Prepared for

California Institute of Technology
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, California

by

Westinghouse Research Laboratories
Beulah Road
Pittsburgh, Pennsylvania 15235

SUMMARY

This report describes continuing work on the design and fabrication of an integrated system which, because of the passive component requirements, includes both silicon diffused devices and tantalum passive components. A design layout for the complete AVDC system is presented which comprises four separated integrated circuit chips combined into one package. Details of the individual chip designs are given and the merit of the 'flip-chip' and conventional assembly methods are compared. The delineation technique used for the tantalum component formation is briefly described.

1. Introduction

The previous interim report presented a design study which from reasons of power dissipation and stability divided the system between six separate silicon chips. By excluding the load resistors from the final output stage it has been possible to reduce the total power dissipation in the system from 2200 milliwatts to 880 milliwatts and this allowed the designs to be consolidated into four separate chips. These are: the reference supply, differential amplifier, transfer generator and output circuit. Furthermore, the layout of the four chips has been organized such that a single chip unit can be made using a simple interconnection overlay mask in the event that four adjacent chips on the same slice are all functioning correctly.

2. Integrated System Design

A design layout for the complete AVDC system was made giving the relative position of each chip and fixing the paths of leads that must be made for interconnection. The overall layout of the system is shown in Figure 1, the exact physical size being slightly less than the original estimate of size. The design is somewhat conservative in allowing 50 mils distance between circuits. This can be reduced to approximately 5 mils in the one chip design. As shown, the final encapsulation must consist of a six terminal, flip-chip type package capable of dissipating the 900 mw produced in the overall circuit. The layout has been made such that a complete one-chip mask can be produced once the individual desired characteristics of each circuit have been obtained.

A final trimming operation on the overall system will be made in two steps to achieve the final output characteristics. First, the tantalum resistor associated with the triangle generator will be trimmed by etching the resistor, while monitoring the generator frequency and obtaining 2.5 kc. The triangle generator, differential amplifier and output circuit can then be mounted flip-chip style on the ceramic substrate, leaving the reference supply unmounted. After it is determined what voltage is required to give the correct symmetry of inputs at the comparator amplifier, the reference supply can be trimmed to this voltage, then mounted in place in the AVDC system. When the single chip AVDC system is made, this operation can be made after the chip is mounted.

3. Design of Individual Circuits

3.1 Reference Supply

The layout and fabrication masks have been made for this circuit with two lots of eight silicon slices being processed for integrated circuits. Diffusions have been carried out on these slices for the isolation step and will be measured for leakage after the B&R masks have been applied. The physical layout is shown in Figure 2.

The background material was chosen to be 1Ω cm n type epitaxial silicon approximately 25 microns thick. This material will yield transistors with a V_{CEO} of 25V, betas greater than 50 and saturation resistances less than 300Ω. Space for a tantalum resistor has been allowed on this chip which will be deposited after the circuit has been checked for operation.

Since the zener diodes should have as near a zero temperature coefficient as possible, the diodes and transistor base regions will be diffused with 200 Ω/□ sheet resistance to give 5.8V reference diodes.

3.2 Differential Amplifier

The layout for this circuit has been completed and is shown in Figure 3. This amplifier will be fabricated on the same background material as used for the reference supply, in addition, floating collector regions will be required because of the two zener voltage specification. The 8.2V zener voltage will be obtained using the P wall boron diffusion and the 14V zener voltage will be obtained using the B&R boron diffusion. The capacitors will then be capable of withstanding 14 volts at the reverse-biased junction. To obtain this 14 volts the transistors are fabricated with 250Ω/□ sheet resistance and 4 microns base depth.

3.3 Triangle Generator

The layout for this chip has also been completed and is shown in Figure 4. This integrated circuit contains the .002 μf tantalum capacitor and 25K resistor account for roughly 75% of the area of the chip. The triangle generator will be fabricated on the same material as the other devices, but will not require a floating collector region under the epitaxial layer. The circuit contains a 14V reference diode requiring that the base of the transisotrs be fabricated with 250Ω/□ sheet resistance at a depth of 4 microns.

3.4 Output Circuit

The layout for this circuit, consisting of the comparator, binary and driver, and output gates is nearly complete and the

fabrication masks will be available soon. This chip will use the same material used for the other circuits and will require floating collector regions to reduce the saturation resistance of the output gates. The output transistors will be capable of 50 ma collector currents.

4. Tantalum Component Fabrication

4.1 Deposition

The triode sputtering system used for the reactive sputtering of tantalum nitride and tantalum oxide components is complete and resistor and dielectric films are now being deposited in this equipment. The deposited film thickness is monitored using the resistance of a standard strip of the sputtered layer.

4.2 Pattern Definition

A method for delineation of the tantalum components which is compatible with the silicon oxide substrate has been evaluated. A comparison was made between using calcium fluoride and aluminum as a transfer mask. This is required since conventional photoresist materials are degraded by the etches required for tantalum. It was found that by delineating the required pattern in an aluminum layer prior to the tantalum deposition and then subsequently removing the aluminum and overlaying tantalum the required component configurations can be achieved.

4.3 Metallization

A metallization scheme which is suitable for both silicon interconnection and tantalum electrodes has been adopted. This utilizes titanium-gold interconnection layers. A vacuum system has been assembled to evaporated the titanium-gold layers. The thickness of the

consecutive layers is monitored by a quartz crystal microbalance. The delineation of these interconnections with conventional photoresist techniques has been examined and is satisfactory.

5. Package Design

5.1 Interconnection Design

As outlined in paragraph 2, the utilization of the same circuit configurations for the four chip layout as for a monolithic design greatly simplifies the lead patterns required in the ceramic substrate of the package for the flip-chip assembly. All the lead terminations have a simple one to one correspondence with the related termination on the adjacent chip so that the intraconnection lead lengths are minimized and no cross-overs are required on the package.

5.2 Thermal Dissipation

The major design problem which arises with the use of the flip chip assembly technique is the thermal dissipation,which is limited in each chip,by the heat which can be removed via the interconnection pads. Since the total area of these pads is much less than the total chip area the thermal resistance for the flip-chip configuration is higher than for a conventional back mounted chip.

A comparative example for the differential amplifier chip, which has the highest power dissipation (300 mw) on the smallest area (80 mil x 75 mil) is given below.

Assuming the possibility of spacing 5 x 5 mil pads at 10 mil intervals for the flip-chip assembly, the maximum number of pads round the periphery is sixteen and the total pad area is 400 $mils^2$ compared

with 6000 $mils^2$ for the total chip area. This reduction in effective heat conductive path together with the additional factor of the transmission of the heat to the pad within the chip itself leads to a working junction temperature of 131.5°C for an 85°C ambient in a worst case analysis for the flip-chip structure compared with a junction temperature of 101.3°C for an 85°C ambient if the chip is totally contacted.

Thus the improvement in reliability gained by avoiding the use of bonded wires in the flip-chip structure may be somewhat deteriorated by the higher junction temperature which may have to be tolerated. However, since a theoretical prediction of thermal resistance is of necessity approximate; experimental determinations of operating junction temperature will be determined for the flip-chip configuration.

6. Program for the Next Report Period

The individual chips for the complete system will be fabricated, tested and assembled into a single package. Performance data and test specifications for the system will be derived.

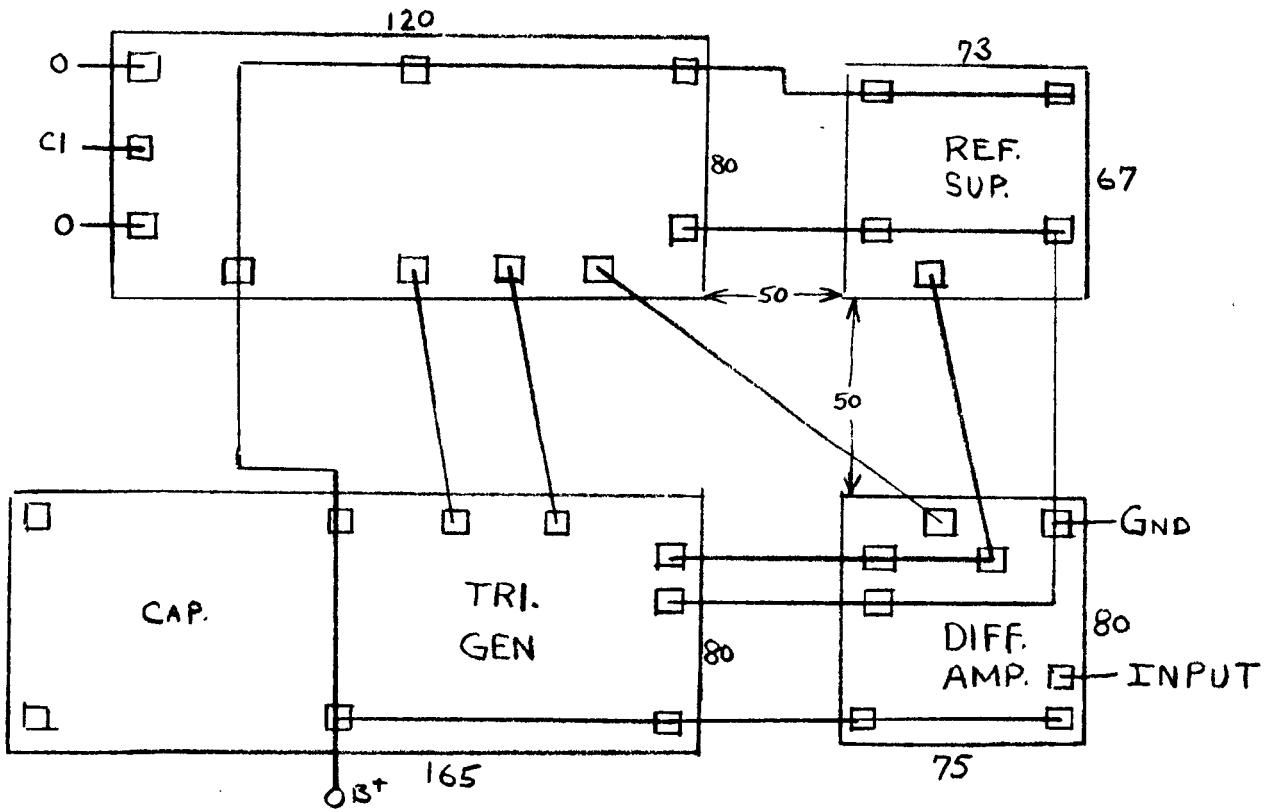

Fig. 1 AVDC System Layout

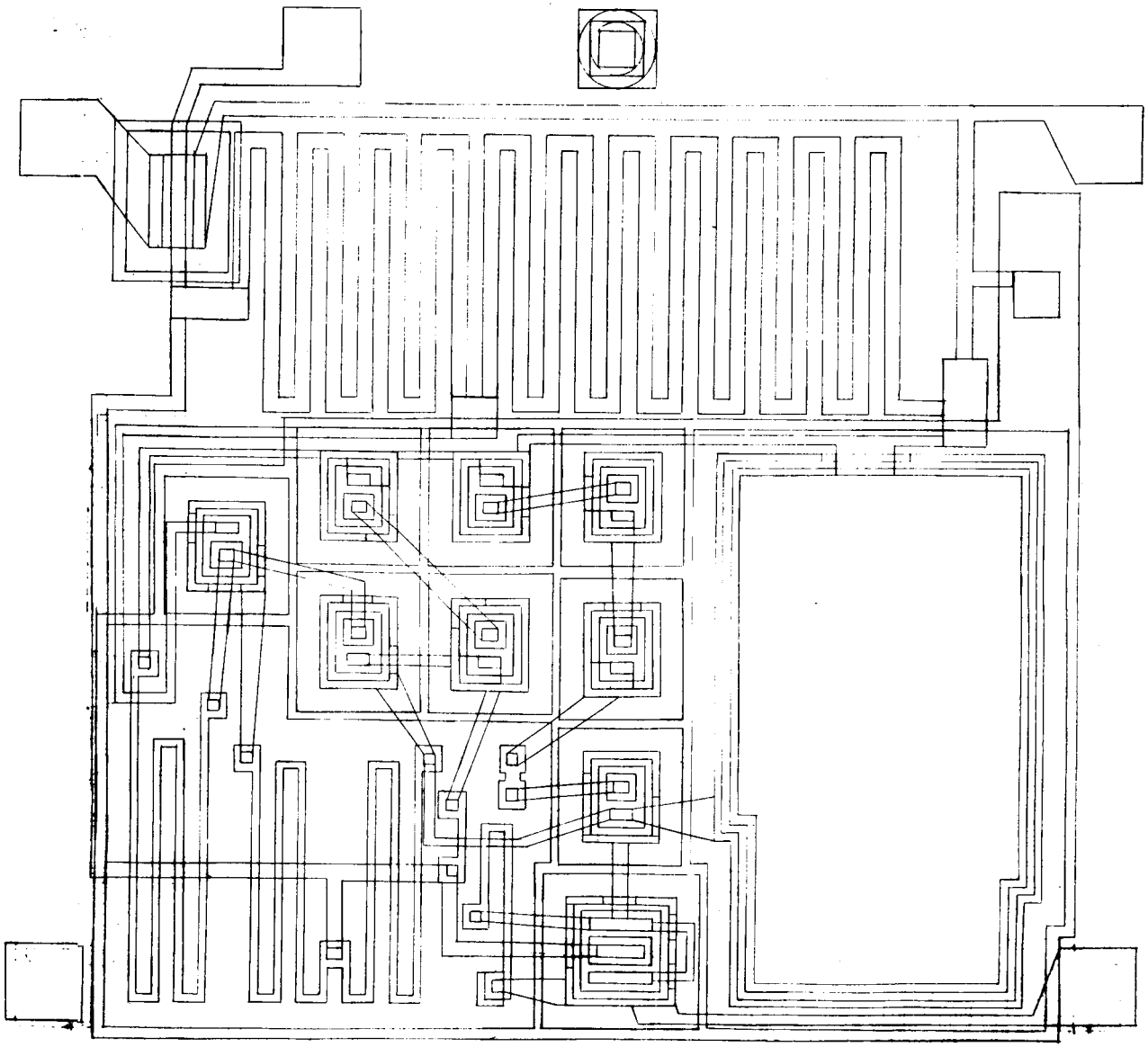

Fig. 2 Reference Supply Layout

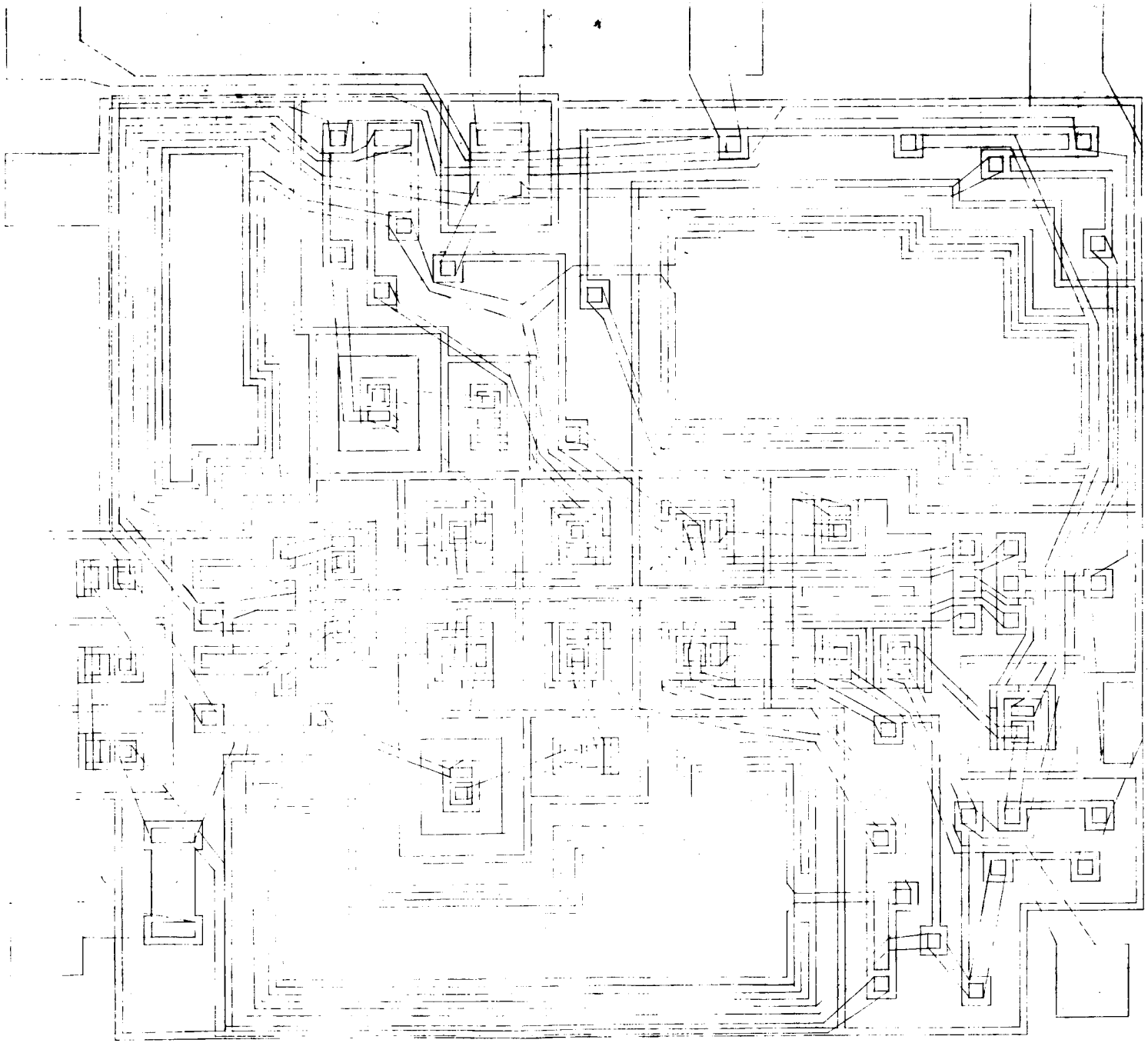

Fig. 3 Differential Amplifier Layout

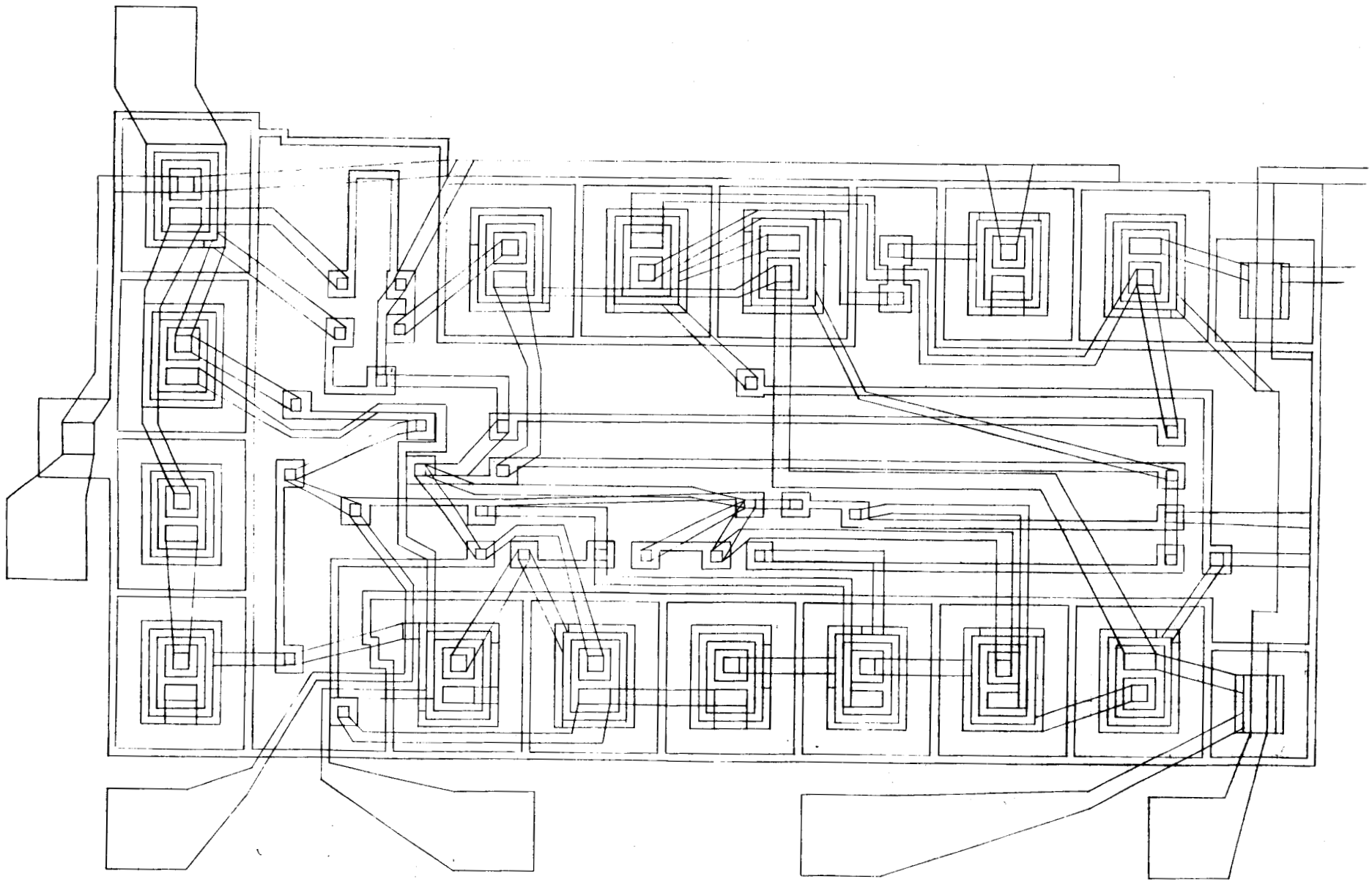

Fig. 4 Triangle Generator Layout